Introduction

The Integrated Circuit is an electronic device which is in great demand for a number of widely varying applications. Its tiny size, replacing conventional components millions of times larger in volume, makes it the ideal building block for computers, control equipment, and other machines requiring switching to be performed quickly, accurately and cheaply. IC's today usually contain 10,000 - 100,000 transistors, fabricated on a 1cm × 1cm chip of monocrystalline silicon. The primary factors limiting the increase in IC size are fabrication defects. For a given chip size to be economically feasible, the probability that a fabricated chip will function properly must be reasonable. This yield percentage is crucial and generally varies exponentially with the chip surface area. Though improvements in silicon crystal growing, photolithographic techniques, etching, diffusion, ion implantation, and impurity reduction are all very important to increasing yield, minimizing area is one improvement which can be made before fabrication. This computational procedure of contorting an IC layout into minimal area without changing its topology or violating design rules (spacing rules which prevent electrical interference) is known as IC layout compaction. Because of the economic advantages of a compact layout, an efficient algorithm for performing automated compaction is very desirable to the semiconductor industry.

Given a functionally correct IC layout, the problem of compacting the circuitry into the smallest area is very difficult to solve in general. Even when compaction is done in one dimension at a time, the problem is complicated. However, with a few restrictions on specifying constraints, the problem is quite manageable. This paper will discuss these simplified problems and their solutions, and look into partial and suboptimal solutions to the more general problems.